REMARKS

The 6 November 2002 official action addressed claims 1-10. Claims 1 and 5-10 are amended. Claims 1-10 are pending for reconsideration.

Drawing amendments

The drawings are amended to use cross-hatching in accordance with MPEP 608.02.

Claim amendments

The claims are amended to recite the additional feature of a semiconductor device provided on a printed circuit board, with the thermal expansion of a thermal expansion buffering sheet being greater than the thermal expansion of the semiconductor device. This feature is disclosed, for example, in Figure 2 of the application and the corresponding text. Further amendments are made to clarify the claim language. No new matter is added.

Prior art rejections

Claims 1-3 and 5-8 were rejected under 35 USC §103(a) as being obvious over Susko (U.S. 6,177,728). Claims 4, 9 and 10 were rejected under §103(a) as being obvious over Susko in view of Buchanan (U.S. 4,963,425). It is believed that the present claims will be seen to be patentably distinguished from the cited references in view of the following discussion.

The claimed invention pertains to printed wiring boards that support semiconductor devices. In accordance with the present claims, a printed wiring board includes a thermal expansion buffering sheet laminated to its surface. The thermal expansion buffering sheet has a lower thermal expansion than the printed wiring board material, and a higher thermal expansion than a semiconductor device provided on the thermal expansion buffering sheet.

Susko's embodiment of Figure 6 teaches providing a thermal expansion buffering sheet 126 on a carrier 128 that is attached to a printed circuit board 32 by solder balls. The purpose of the thermal expansion buffering sheet is to

match the thermal expansion of a chip 12 provided on the carrier 128 (see col. 5, lines 18-22). In Susko's other embodiments the thermal expansion buffering material is laminated within the printed circuit board. In contrast the present claims state that the thermal expansion of the thermal expansion buffering sheet is ***laminated on the surface of a printed circuit board*** and that its thermal expansion is ***greater*** than the thermal expansion of the chip.

Buchanan teaches a printed circuit board in which a thermal expansion buffer 20 is laminated ***within*** a fiber reinforced board 10 and has a lower coefficient of thermal expansion than the fiber reinforced board. Buchanan teaches nothing about laminating a thermal expansion buffering layer on the surface of a printed circuit board.

Accordingly, neither reference teaches a printed wiring board that includes a thermal expansion buffering sheet laminated to its surface, with the thermal expansion buffering sheet having a lower thermal expansion than the printed wiring board material and a higher thermal expansion than a semiconductor device provided on the thermal expansion buffering sheet. Each of the independent claims recites these features and is therefore distinguished on those bases, as are the dependent claims which are distinguished for those reasons as well as for their additional novel features.

The foregoing amendments and remarks address all bases for objection and rejection and are believed to place the case in condition for allowance. The examiner is invited to contact the undersigned to resolve any remaining issues.

Respectfully submitted,

By 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Shigeru MORI
Title:	PRINTED WIRING BOARD
Application No.:	09/812,817
Filing Date:	03/21/2001
Examiner:	PATEL, Ishwarbhai B.
Art Unit:	2827

VERSION SHOWING CHANGES MADE IN REPLY TO OFFICIAL ACTION OF 6 NOVEMBER 2002 UNDER 37 CFR §1.111

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Sir:

In reply to the official action mailed 6 November 2002, the application is amended as follows:

In the claims:

1. (Amended) A printed wiring board comprising:

a printed wiring substrate having a plurality of ~~a~~ wiring layers;~~, and~~

a thermal expansion buffering sheet is integrally laminated on a surface of said printed wiring substrate and having a lower coefficient of thermal expansion than that of said printed wiring substrate~~, which is integrally laminated on a surface of said printed wiring substrate~~; and

a semiconductor device provided on the thermal expansion buffering sheet,

wherein the thermal expansion buffering sheet has a higher coefficient of thermal expansion than the semiconductor device.

5. (Amended) A printed wiring board according to claim 1, ~~wherein~~ further comprising an electrode pattern ~~so as to~~ on a surface of said thermal expansion buffering sheet connecting ~~a part to be mounted on a surface~~ the semiconductor device to a wiring section of said printed wiring board ~~is provided on a surface of said thermal expansion buffering sheet~~.

6. (Amended) A printed wiring board according to claim 5, wherein ~~said part to be mounted on said surface of said printed wiring board~~the semiconductor device is connected to said electrode pattern via a solder ball.

7. (Amended) A printed wiring board comprising:

a multi-layer wiring section which laminates wiring layers and insulation layers alternately;~~,~~

a thermal expansion buffering sheet is integrally laminated on a surface of said multi-layer wiring section and having a lower coefficient of thermal expansion than that of said multi-layer wiring section~~, which is integrally laminated on a surface of said multi-layer wiring section~~; and

a semiconductor device provided on the thermal expansion buffering sheet,

wherein the thermal expansion buffering sheet has a higher coefficient of thermal expansion than the semiconductor device.

8. (Amended) A printed wiring board comprising:

a multi-layer wiring section which laminates wiring layers and insulation layers alternately;~~,~~

a thermal expansion buffering sheet integrally laminated on a surface of said multi-layer wiring section and having a lower coefficient of thermal

expansion than that of said multi-layer wiring section~~, which is integrally laminated on a surface of said multi-layer wiring section~~; ~~, and~~

a semiconductor device provided on the thermal expansion buffering sheet; and

an electrode pattern provided on a surface of said thermal expansion buffering sheet ~~so as to~~ connecting ~~a part to be mounted on a surface of said printed wiring board~~the semiconductor device to the multi-layer wiring section,

wherein the thermal expansion buffering sheet has a higher coefficient of thermal expansion than the semiconductor device.

9. (Amended) A printed wiring board comprising:

a multi-layer wiring section which laminates wiring layers and insulation layers alternately; ~~,~~

a thermal expansion buffering sheet, a material of which is aramid, integrally laminated on a surface of said multi-layer wiring section and having a lower coefficient of thermal expansion than that of said multi-layer wiring section~~, which is integrally laminated on a surface of said multi-layer wiring section~~; and

a semiconductor device provided on the thermal expansion buffering sheet,

wherein the thermal expansion buffering sheet has a higher coefficient of thermal expansion than the semiconductor device.

10. (Amended) A printed wiring board comprising:

a multi-layer wiring section which laminates wiring layers and insulation layers alternately; ~~,~~

a thermal expansion buffering sheet, a material of which is aramid, integrally laminated on a surface of said multi-layer wiring section and having a lower coefficient of thermal expansion than that of said multi-layer wiring section~~, which is integrally laminated on a surface of said multi-layer wiring section~~; ~~,~~

a semiconductor device provided on the thermal expansion buffering sheet; and

an electrode pattern provided on a surface of said thermal expansion buffering sheet ~~so as to~~ connecting ~~a part to be mounted on a surface of said printed wiring board~~the semiconductor device to the multi-layer wiring section,

wherein the thermal expansion buffering sheet has a higher coefficient of thermal expansion than the semiconductor device.